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WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit device fabricated on a semiconductor substrate of one conductivity type, comprising:
 - shallow trench isolating regions having a first depth, and formed in surface portions of said semiconductor substrate for defining active areas therebetween;
 - a terminal formed on said semiconductor substrate, and unavoidably applied with static charge;
 - a circuit component of an integrated circuit formed in one of said active areas, and connected between said terminal and a first source of constant voltage; and
 - a protection circuit protecting said circuit component from said static charge, formed in at least said one of said active areas, and including
 - a first impurity region of said one conductivity type formed under said at least one of said active areas and serving as a base region of a bipolar transistor,
 - a second impurity region of the other conductivity type opposite to said one conductivity type formed in a surface portion of said first impurity region, connected to said terminal and serving as one of an emitter region and a collector region of said bipolar transistor and
 - a third impurity region of said other conductivity type connected to said first source of constant voltage, formed in another surface portion of said semiconductor substrate in such a manner that static charge flows through

said first impurity region without substantial resistance due to said shallow trench isolating regions and serving as the other of said emitter region and said collector region of said bipolar transistor.

2. The semiconductor integrated circuit device as set forth in claim 1, in which said third impurity region has

a first impurity sub-region formed in a surface portion of another active area adjacent to said one of said active areas and

a second impurity sub-region contiguous to a bottom surface of said first impurity sub-region and extending in said first impurity region under said second impurity region.

3. The semiconductor integrated circuit device as set forth in claim 2, in which said first impurity sub-region has a first portion contiguous to said second impurity sub-region and a second portion heavier in dopant concentration than said first portion and connected to said first source of constant voltage.

4. The semiconductor integrated circuit device as set forth in claim 2, in which said circuit component is a field effect transistor having source and drain regions of said other conductivity type formed in said one of said active areas, and one of said source and drain regions serves as said second impurity region.

5. The semiconductor integrated circuit device as set forth in claim 1, in which said third impurity region has

a first impurity sub-region formed in another surface portion of said first impurity region spaced from said second impurity region and

a second impurity sub-region contiguous to a bottom surface of said first impurity sub-region and extending in said first impurity region under said second impurity region.

6. The semiconductor integrated circuit device as set forth in claim 5, in which said first impurity sub-region has a first portion contiguous to said second impurity sub-region and a second portion heavier in dopant concentration than said first portion and connected to said first source of constant voltage.

7. The semiconductor integrated circuit device as set forth in claim 5, in which said circuit component is a field effect transistor having source and drain regions of said other conductivity type formed in said one of said active areas, one of said source and drain regions serves as said second impurity region, and the other of said source and drain regions serves as said first impurity sub-region.

8. The semiconductor integrated circuit device as set forth in claim 1, in which said third impurity region is formed in another active area adjacent to said one of said active areas and having a second depth greater than said first depth.

9. The semiconductor integrated circuit device as set forth in claim 8, in which said circuit component is a field effect transistor having source and drain regions of said other conductivity type formed in said one of said active areas, and one of said source and drain regions serves as said second impurity region.

10. The semiconductor integrated circuit device as set forth in claim 1, in which said third impurity region is formed in another surface portion of said first impurity region and deeper than said second impurity region.

11. The semiconductor integrated circuit device as set forth in claim 10, in which said circuit component is a field effect transistor having source and drain regions of said other conductivity type formed in said one of said active areas, one of said source and drain regions serves as said second impurity region, and the other of said source and drain region serves as a part of said third impurity region.

12. The semiconductor integrated circuit device as set forth in claim 1, in which said third impurity region extends in said first impurity region under said second impurity region.

13. The semiconductor integrated circuit device as set forth in claim 10, in which said circuit component is a field effect transistor having source and drain regions of said other conductivity type formed in said one of said active areas, and one of said source and drain regions serves as said second impurity region.

14. The semiconductor integrated circuit device as set forth in claim 1, in which said terminal serves as a signal output terminal, and said circuit component is an output transistor.

15. The semiconductor integrated circuit device as set forth in claim 1, in which said terminal serves as a signal input and output terminal, and said cir-

cuit component is an output transistor forming a part of an input and output circuit connected to said terminal.

16. A process for fabricating a semiconductor integrated circuit device, comprising the steps of:

- a) preparing a semiconductor substrate having one conductivity type;
- b) introducing a first dopant impurity into a surface portion of said semiconductor substrate for forming a first impurity region of the other conductivity type opposite to said one conductivity type;
- c) introducing a second dopant impurity into a surface portion of said first impurity region for forming a second impurity region shallower than said first impurity region and having said one conductivity type;
- d) forming a groove shallower than said second impurity region in a surface portion of said second impurity region;
- e) filling said groove with insulating material for forming a shallow trench isolating region; and
- f) introducing a third dopant impurity into another surface portion of said second impurity region for forming a third impurity region of said one conductivity type shallower than said second impurity region, said first impurity region, said second impurity region and said third impurity region serving as an emitter region, a base region and a collector region of a vertical bipolar transistor for discharging static charge current applied to a terminal connected to said third impurity region.

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